

PTO/SB/08B (02-03)

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Substitute for form 1448/PTO SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete If Known	
				Application Number	10/749,096
				Filing Date	December 30, 2003
				First Named Inventor	Rafael Reif
				Art Unit	3745
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	MIT-136DUS
Sheet	2	of	2		

[illegible]

Examiner Signature	<i>Dwight K. Owen</i>	Date Considered	1/6/05
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Signature W. Hughes N. - [Signature] Continued

*EXAMINER: Include if reference considered, whether or not citation is in conformance with MPEP 618. Draw line through citation if not in conformance and not considered. Initial copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEE'S OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22315-1450.

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Sheet	1	of	2
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PTO/SB/08A (02-03)

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Complete if Known

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First Named Inventor	Rafael Reif
Art Unit	3745
Examiner Name	Not Yet Assigned
Attorney Docket Number	MIT-136DUS

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)	MM-DD-YYYY			
DE		2 645 681	04/07/1989	Thomson CSF		
DE		WO 02/09182 A1	01/31/2002	Christian Val		

Examiner Signature	<i>Daniel K. O...</i>	Date Considered	1/6/05
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.

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PTO/SB/088 (02-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/749,096
				Filing Date	December 30, 2003
				First Named Inventor	Rafael Reif
				Art Unit	3745
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	MIT-136DUS

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DR		Y. HAYASHI, Fabrication of Three Dimensional IC Using "Cumulatively Bonded IC" (CUBIC) Technology Symposium on VLSI Technology, 1990, pages 95-96	
		PCT/US/03/41514 International Search Report June 17, 2004	

Examiner Signature	<i>Douglas H. Owen</i>	Date Considered	1/6/05
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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PTO/88/088 (02-03)

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		Application Number	10/749,096
		Filing Date	December 30, 2003
		First Named Inventor	Rafael Reif
		Art Unit	3745
		Examiner Name	Not Yet Assigned
Attorney Docket Number	MIT-136DUS		
Sheet	1	of	1

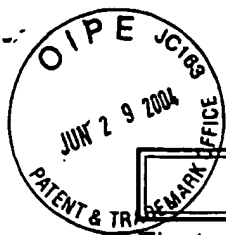
OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
Dko		OSAMU TABATA, Anisotropic Etching of Silicon in TMAH Solutions, Toyota Central Research and Development Laboratories, Inc., February 21, 1992, Pages 51-57, Japan	
Dko		PHILIP M. SAILER, Creating 3D Circuits Using Transferred Films, Circuits & Devices, November 1997, Pages 27-30	
Dko		TAKUJI MATSUMOTO, New Three-Dimensional Wafer Bonding Technology Using the Adhesive Injection Method, March, 1998, Pages 1217-1221, Jpn. J. Appl. Phys. Vol. 37 (1998)	
Dko		A. FAN, Copper Wafer Bonding, Electrochemical and Solid-State Letters, 1999, Pages 534-536, Cambridge, Massachusetts	
		ARIFUR RAHMAN, Wire-Length Distribution of Three-Dimensional Integrated Circuits, 1999, Pages 233-235	
Dko		VICTOR W.C. CHAN, Three Dimensional CMOS Integrated Circuits on Large Grain Polysilicon Films, EEE, Hong Kong University of Science and Technology, 2000, Pages 00-161 - 00-164 Hong Kong	
Dko		K.W. LEE, Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology, Dept. of Machine Intelligence and Systems Engineering, 2000, Pages 00-165 - 00-168, Hong Kong	
Dko		KUAN-NENG CHEN, Microstructure Examination of Copper Wafer Bonding, Microsystem Technology Laboratories, December 20, 2000, Pages 331-335, Cambridge, Massachusetts	

Examiner Signature	<i>Dough K. Oma</i>	Date Considered	1/6/05
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










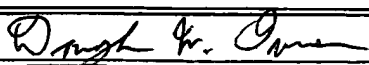
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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	MULTI-LAYER INTEGRATED SEMICONDUCTOR STRUCTURE HAVING AN ELECTRICAL SHIELDING PORTION						
Application Number: 10/749096							
Confirmation Number: 3177							
First Named Applicant: Rafael Reif							
Attorney Docket Number: MIT-136DUS							
Art Unit: 3745							
Search string: (4313126 or 4402761 or 4456888 or 4599704 or 4986861 or 5156997 or 5206186 or 5445994 or 5821138 or 5923087 or 6441478).pn.							
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	4313126	1982-01-26	Krumm et al.			
	2	4402761	1983-09-06	Feist			
	3	4456888	1984-01-26	Ayasli			
	4	4599704	1986-07-08	Mazin			
	5	4986861	1991-01-22	Nishida et al.			
	6	5156997	1992-10-20	Kumar et al.			
	7	5206186	1993-04-27	Neugebauer et al.			
	8	5445994	1995-08-29	Gilton			
	9	5821138	1998-10-13	Yamazaki et al.			
	10	5923087	1999-07-13	Suzuki et al.			
	11	6441478	2002-08-27	Park			
Signature							
Examiner Name					Date		
					1/6/05		